What is claimed is:

1. A liquid crystal display device having a liquid crystal display panel, a plurality of liquid crystal drive circuits formed over an edge portion of the liquid crystal display panel, and a plurality of signal lines formed over the edge portion of the liquid crystal display panel for transmitting an image signal and an external clock signal between respective drive circuits,

wherein the liquid crystal drive circuit comprises:

an image signal input circuit connected with the signal line;

a clock control circuit connected with the signal line, and generating an internal clock signal based on the external clock signal;

the internal clock signal swinging from a first voltage to a second voltage lower than the first voltage;

a data storage circuit for storing an image signal at a timing of a voltage changing from a first voltage to a second voltage or at a timing of a voltage changing from a second voltage to a first voltage of the internal clock signal;

a voltage select circuit for selecting a voltage for driving the liquid crystal display panel; and

an output circuit for outputting the external clock signal to next liquid crystal drive circuit, and having a clock compensation circuit.

2. The liquid crystal display device as claimed in Claim 1, wherein the clock compensation circuit is operable to correct a duty ratio of the external clock.

3. The liquid crystal display device as claimed in Claim 1, wherein the clock compensation circuit has an inverter.

4. The liquid crystal display device as claimed in Claim 1, wherein the clock compensation circuit has a phase locked loop circuit.

5. The liquid crystal display device as claimed in Claim 1, wherein the clock compensation circuit has a delay locked loop circuit.

6. A liquid crystal display device having a liquid crystal display element and liquid crystal drive circuit formed over the liquid crystal display element, a plurality of signal lines formed over an edge portion of the liquid crystal display element for transmitting a signal between the drive circuits,

wherein the liquid crystal drive circuit comprises:

a data input terminal connected with the signal line, and an image signal being input thereto;

a clock control circuit for inputting an external clock and outputting an internal clock, the internal clock having a first period for permitting output of a first voltage and a second period for output of a second voltage;

a data latch circuit for taking thereto an image signal at a timing of a voltage changing from a first voltage to a second voltage or at a timing of a voltage changing from a second voltage to a first voltage of the internal clock;

a data bus for output of the image signal from the data latch circuit;

a voltage output circuit for outputting a voltage according to the image signal on the data bus to the liquid crystal display element;

a data output circuit for outputting the image signal on the data bus to a next stage of liquid crystal drive circuit; and

a clock formation circuit being operable to correct a duty ratio of the external clock.

7. The liquid crystal display device as claimed in Claim 6, wherein the clock formation circuit has an inverter.

8. The liquid crystal display device as claimed in Claim 6, wherein the clock formation circuit has a phase locked loop circuit.

9. The liquid crystal display device as claimed in Claim 6, wherein the clock formation circuit has a delay locked loop circuit.

10. The liquid crystal display device as claimed in Claim 6, wherein the data bus comprises tow systems of signal lines.